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=> s 395/?/ccls
L3       38673 395/?/CCLS

=> s l1 and (integrated (2W) circuit?)/ab
         28302 INTEGRATED/AB
        188261 CIRCUIT?/AB
         15455 (INTEGRATED (2W) CIRCUIT?)/AB
L4       15294 L1 AND (INTEGRATED (2W) CIRCUIT?)/AB

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L1        15294 S (INTEGRATED (1W) CIRCUIT?)/AB
L2           22 S L1 AND (MANUFACTUR? (2W) SAME (2W) PROCESS?)
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L3        38673 S 395/?/CCLS
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     (FILE 'USPAT' ENTERED AT 09:27:26 ON 09 OCT 1997)
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L1        15294 S (INTEGRATED (1W) CIRCUIT?)/AB
L2           22 S L1 AND (MANUFACTUR? (2W) SAME (2W) PROCESS?)
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L3        38673 S 395/?/CCLS
L4        15294 S L1 AND (INTEGRATED (2W) CIRCUIT?)/AB

=> d kwic l2 1-22

US PAT NO:     5,604,828 [IMAGE AVAILABLE]            L2: 1 of 22

ABSTRACT:
An optical integrated circuit provides multiple power splitting functions
and comprises a plurality of optical power splitters networked together. In
one embodiment, the optical integrated circuit has two 2.times.2 optical
power splitters ganged together such that the circuit simultaneously provides
two different 1.times.2 power splitting functions and four different
1.times.3 power splitting functions. In another embodiment, the optical
integrated circuit has three 2.times.2 optical power splitters ganged
together such that the circuit simultaneously provides two 1.times.2 power
splitting functions, four 1.times.3 power splitting functions, and two
1.times.4 power splitting functions. Since each integrated circuit
provides more than one power splitting function, the integrated circuit
is more versatile than a single power splitter. The integrated circuit
may also present a lower cost in comparison to a circuit formed with discrete
elements since additional power splitters can be placed on a single substrate
for only a nominal increase in cost. The integrated circuit further
reduces the time needed to couple fibers to their respective power splitters
since multiple fibers in a fiber ribbon array can be simultaneously coupled
to the ports of the optical integrated circuit.

DETDESC:
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DETD(11)

While . . . be fabricated in any suitable manner. With planar waveguide circuit technology, the desired splitters as well as their interconnections are **manufactured** during the **same process**, analogous to integrated electronic circuits. The planar waveguide circuit technology is advantageous to discrete components when multiple splitters are used. . .

US PAT NO: 5,596,219 [IMAGE AVAILABLE] L2: 2 of 22

ABSTRACT:
Semiconductor component with monolithically **integrated** electronic **circuits** and monolithically integrated sen
sor/acutator, whereby the
sensor/actuator is manufactured with methods of surface micromachining in a sensor layer (3) of. . .

DETDESC:

DETD(6)

The . . . in this example of a sensor layer 3 of, for example, polysilicon structured with sensor webs 6 and being advantageously **manufactured** in the **same process** steps together with the gate electrodes. The sensor webs 6 are connected to one another and, for example, form a. . .

US PAT NO: 5,572,114 [IMAGE AVAILABLE] L2: 3 of 22

ABSTRACT:
A semiconductor **integrated circuit** for performing a current mirror function and capable of operating stably at a low supply voltage to yield an output. . .

DETDESC:

DETD(92)

Furthermore, the current mirror circuit provided by the present invention can be **manufactured** with the **same processes** as are used for the conventional current mirror circuit, without requiring additional processing steps for the vertical type transistor.

US PAT NO: 5,570,043 [IMAGE AVAILABLE] L2: 4 of 22

ABSTRACT:
An overvoltage tolerant output buffer circuit for coupling an **integrated circuit** (IC) to externa
l electrical apparatus by way of a contact pad or
other input/output connection. An overvoltage protection circuit is. . .

SUMMARY:

BSUM(4)

An . . . tolerant of voltages on the I/O connections thereof which are different from voltages which may be received from a circuit **manufactured** using the **same** fabrication **process**.

US PAT NO: 5,485,124 [IMAGE AVAILABLE] L2: 5 of 22

ABSTRACT:
The . . . pair circuit in the auxiliary amplifier. Both resistance ratios and ratios between complete circuits can be realised highly accurately in **integrated circuits**. As a result, the accuracy of the gain factor is great. In an embodiment of the invention the dimensions of. . .

DETDESC:

DETD(6)

Since . . . the transistors in the long-tailed pair circuit 6-1 in the auxiliary amplifier 2. Since the resistors R1 and R2 are **manufactured** in a **same process**, their ratio is accu
rately reproducible. Ratios of complete
circuits are likewise accurately reproducible on-chip, so that the invention provides an. . .

US PAT NO: 5,412,234 [IMAGE AVAILABLE] L2: 6 of 22

ABSTRACT:
It . . . possible to limit the voltage across a diode to the level of the pinch-off voltage of a JFET in an **integrated circuit** by connecting the diode in series with the JFET. As a result, the voltage offered through the JFET can be. . . is coupled to the diode. The diode with the JFET occupies very little space and can be readily incorporated in **integrated circuit** designs.

DETDESC:

DETD(11)

To . . . sufficiently low doping (for example, approximately 10.sup.12 atoms per cm.sup.2). In other cases, for example, when the zone 19 is **manufactured** in the **same process** steps as a zone of one of the circuit elements, a higher doping concentration may be desirable and it may. . .

US PAT NO: 5,394,104 [IMAGE AVAILABLE] L2: 7 of 22

ABSTRACT:
A power-on reset circuit is provided which holds an **integrated circuit** device in a reset mode until at least two conditions are satisfied: supply voltage Vcc must be above a specified. . .

DETDESC:

DETD(19)

Sense amplifiers PORSA1 and PORSA2 are **manufactured** by the **same process** and with the same sizes as other sens
e amplifiers in the chip.
Therefore they will begin to operate properly when. . .

CLAIMS:

CLMS(8)

8. . . .
second detect signals and providing an output signal,

wherein said means for providing a second detect signal comprises two sense amplifiers **manufactured** by the **same process** and with the same component sizes as sense amplifiers elsewhere in said integrated circuit, said sense amplifiers providing said second. . .

US PAT NO: 5,361,229 [IMAGE AVAILABLE] L2: 8 of 22

ABSTRACT:
The bit line for reading data in or writing data out from a CMOS **integrated circuit** latch is pre
charged to the trip point voltage of the latch (as
determined by the latch's transistor design) shortly before. . .

SUMMARY:

BSUM(15)

In . . . read operation. This eliminates read disturb and ensures accurate latch data reading and writing. The precharge circuit uses an inverter **manufactured** by the **same process** and having corresponding characteristics to the inverters in the latch circuit. This precharge inverter has its input and output shorted. . .

US PAT NO: 5,355,123 [IMAGE AVAILABLE] L2: 9 of 22

ABSTRACT:
An arrangement for detecting overheating of a power **integrated circuit** includes a power device integrated in a semiconductor substrate and an overheating detection circuit. The overheating detection circuit includes a. . .

DETDESC:

DETD(13)

FIG. . . . the MOSFET consisting of n- type region 15, n+ type region 17, 18 and the gate electrode 22 can be **manufactured** through the **same process** steps as in FIG. 3. In addition, the embo
diments of the present
invention shown in FIG. 3 and FIG. 9. . .

US PAT NO: 5,349,336 [IMAGE AVAILABLE] L2: 10 of 22

ABSTRACT:
An arrangement for detecting overheating of a power **integrated circuit** includes a power device integrated in a semiconductor substrate and an overheating detection circuit. The overheating detection circuit includes a. . .

DETDESC:

DETD(13)

FIG. . . . the MOSFET consisting of n- type region 15, n+ type region 17, 18 and the gate electrode 22 can be **manufactured** through the **same process** steps as in FIG. 3. In addition, the embo
diments of the present
invention shown in FIG. 3 and FIG. 9. . .

US PAT NO: 5,239,216 [IMAGE AVAILABLE] L2: 11 of 22

ABSTRACT:
A semiconductor **integrated circuit** includes a current source for supplying a current i, a resistor, a switch having a control end connected to the. . .

DETDESC:

DETD(24)

The resistor R1 and R3 are of the same structure and have been simultaneously **manufactured** by the **same process**. Hence, their resistances are different from the respective design values, by substantially the same amount. If the resistance of the. . .

US PAT NO: 5,239,208 [IMAGE AVAILABLE] L2: 12 of 22

ABSTRACT:
A semiconductor **integrated circuit** including a constant current circuit or an active load circuit, which includes two field effect transistors having the same type. . .

DETDESC:

DETD(36)

As . . . appropriately setting the gate length of the FET, FETs having more than two levels of threshold voltage can be simultaneously **manufactured** at the **same** manufacturing **process** thereof. As a result, with respect to Table 1, the gate length of the FET Q.sub.3 and that of the. . .

US PAT NO: 5,138,437 [IMAGE AVAILABLE] L2: 13 of 22

ABSTRACT:
A semiconductor **integrated circuit** device comprises a general purpose unit having a general purpose function and a specific unit for a specific use of the semiconductor **integrated circuit** device. In addition, the semiconductor **integrated circuit** device has structure in which a plurality of layers each having an **integrated circuit** formed therein are stacked in a three-dimensional manner. Specific unit layers are formed on the surface of the layer having. . .

SUMMARY:

BSUM(11)

According . . . users for the semiconductor integrated circuit device are various in kind, only the general purpose unit layer can be efficiently **manufactured** in the **same** manufacturing **processes**. In particular, when the general purpose unit is formed in a first layer, the general purpose unit can be manufactured. . .

DETDESC:

DETD(5)

As . . . therein are separated to form the mixed LSI, so that only at least the general purpose unit can be efficiently **manufactured** in the **same** manufacturing **process** even if the mixed LSI is va

rious in kind,
whereby the manufacturing period can be shortened.

US PAT NO: 5,016,986 [IMAGE AVAILABLE] L2: 14 of 22

ABSTRACT:
In a liquid crystal display apparatus, in order to reduce the size and weight, an **integrated circuit** for driving a liquid crystal is mounted on the glass substrate including the liquid crystal panel either directly or by. . . and liquid crystal display is effected in this region. Further, in the non-overlapping region of the two glass substrates, the **integrated circuit** is connected either d
irectly or by way of a tape carrier. On the
glass substrates, electrodes for varying the optical characteristics of the liquid crystals are provided, and the **integrated circuit** drives the liquid crystal by controlling the voltage applied to the electrodes. Further transparent insulation films are formed usually formed. . . may be selectively formed on the portions where defective insulation is likely to occur between the wiring conductors following the **integrated circuit** from the electrodes, or between the **integrated circuit** and the peripheral portion of the connecting part.

DETDESC:

DETD(33)

FIG. . . . is that the output electrode 34a and transparent insulation layer 41a do not overlap. The output conductor 33a which is **manufactured** in the **same process** as the output ele
ctrode 34a and extends in the display
region from the output electrode 34a is overlapping with the. . .

US PAT NO: 4,770,242 [IMAGE AVAILABLE] L2: 15 of 22

ABSTRACT:
A cooling device for providing cooling of **integrated circuit** semiconductor chips is so arranged as to transfer a heat via thin fin members which are fitted with each other. . .

DETDESC:

DETD(14)

FIG. . . . inner surface of the housing 43. Since, in this embodiment, both the thermal conductive members 17 and 44 can be **manufactured** in the **same process** of manufacture, it is po
ssible easily to manufacture the
fins 16 and 45 with the same precision. Further, the productivity. . .

US PAT NO: 4,627,082 [IMAGE AVAILABLE] L2: 16 of 22

ABSTRACT:
The invention relates to an **integrated** MOS **circuit** comprising a MOS transistor which is connected as a resistor and which, when conducting current, generates a voltage which is. . .

DETDESC:

DETD(12)

The . . . threshold voltage. Since this threshold voltage exhibits a fairly large spread, the transistor 25 is incorporated. This transistor, which is **manufactured** by the **same** **processing** steps as the transistor 20 and will therefore exhibit the same spread in threshold voltage, is switched so that the. . .

US PAT NO: 4,595,942 [IMAGE AVAILABLE] L2: 17 of 22

ABSTRACT:
A compact **integrated** logic **circuit** having an inverter transistor and several coupling diodes adjoining the collector region of said transistor. Current is applied to the. . .

DETDESC:

DETD(27)

The . . . integrated circuits is considerably simpler than for the described known circuit. The integrated circuit according to the invention can be **manufactured** with the **same** available **process** in which, for example, LS TTL and I.sup.2 L can also be manufactured. In contrast with the known circuit described,. . .

US PAT NO: 4,532,530 [IMAGE AVAILABLE] L2: 18 of 22

ABSTRACT:
A . . . The resistor material is heavily doped polycrystalline silicon which can be formed on the same process lines with those for **integrated** **circuits** to reduce equipm
ent costs and achieve higher yields. Glass mesas
thermally isolate the active portion of the resistor from the. . .

DETDESC:

DETD(7)

The advantages of the above invention structure are threefold. First, it can be **manufactured** on the **same** **process** line with integrated circuits to reduce equipment costs and achieve high yields. Second, the glass mesa 43 provides the appropriate. . .

DETDESC:

DETD(24)

In . . . an improved bubble jet ink printing system having bubble generating resistors that have long operating lifetimes. The resistors can be **manufactured** on the **same** **process** lines with those for integrated circuits to reduce equipment costs and achieve high yields. The glass mesa structures allows the. . .

US PAT NO: 4,419,745 [IMAGE AVAILABLE] L2: 19 of 22

ABSTRACT:
An improvement of a semiconductor **integrated** **circuit** device of a memory cell array which is formed by integrated injection logic memory cells. The semiconductor **integrated** **circuit** includes integration injection logic memory cells which are arranged in matrix form, word lines and bit lines which are connected. . .

DETDESC:

DETD(12)

In . . . bit lines B.sub..0. and B.sub.1, because in this area, the current-source transistors Q.sub.7 are provided. Therefore, in this area, lines **manufactured** by the **same process** as that used in manufacturing the bit lines can be used as the bias lines 1.sub.5 and 1.sub.6. Further, according. . .

US PAT NO: 4,135,295 [IMAGE AVAILABLE] L2: 20 of 22

ABSTRACT:
Selected circuit elements and interconnections of an **integrated circuit** device are connected by platinum silicide fuse links which open when electrical power exceeds a threshold amount. The fuse is. . .

SUMMARY:

BSUM(8)

Because . . . of the prior art, and had lower fusing current than polycrystalline silicon fuses of the prior art and could be **manufactured** in the **same processing** step as other int
egrated circuit devices or portions
thereof.

US PAT NO: 4,042,950 [IMAGE AVAILABLE] L2: 21 of 22

ABSTRACT:
Selected circuit elements and interconnections of a **integrated circuit** device are connected by platinum silicide fuse links which open when electrical power exceeds a threshold amount. The fuse is. . .

SUMMARY:

BSUM(8)

Because . . . of the prior art, and had lower fusing current than polycrystalline silicon fuses of the prior art and could be **manufactured** in the **same processing** step as other int
egrated circuit devices or portions
thereof.

US PAT NO: 3,772,536 [IMAGE AVAILABLE] L2: 22 of 22

ABSTRACT:
There is disclosed an article and method of fabrication thereof comprising an **integrated** semiconductor **circuit** in the form of a digital cell of standard configuration suitable for universal use in large scale **integrated circuit** arrays which
may be mass produced up to the final interconnecting
metallization step and thereafter stored for use in filling. . .

DETDESC:

DETD(2)

Although . . . digital cell which forms the subject matter of the invention will be described. Such an actual cell is, of course,

manufactured by the **same process** as that used for a single cell, the only difference being in the complexity of the structures, which aspect will.
. .

=> d l2 1-22

1. 5,604,828, Feb. 18, 1997, Multi-purpose optical integrated circuit; Henry H. Yaffe, 385/14; 359/114, 115; 385/24, 48 [IMAGE AVAILABLE]

2. 5,596,219, Jan. 21, 1997, Thermal sensor/actuator in semiconductor material; Christofer Hierold, 257/467, 415 [IMAGE AVAILABLE]

3. 5,572,114, Nov. 5, 1996, Current mirror circuit with bipolar transistor connected in reverse arrangement; Kouzou Ichimaru, 323/315, 316 [IMAGE AVAILABLE]

4. 5,570,043, Oct. 29, 1996, Overvoltage tolerant intergrated circuit output buffer; Jonathan F. Churchill, 326/81, 21, 27 [IMAGE AVAILABLE]

5. 5,485,124, Jan. 16, 1996, Integrated amplifier with an accurately defined gain factor; Jacob Mulder, 330/278, 254 [IMAGE AVAILABLE]

6. 5,412,234, May 2, 1995, Integrated semiconductor circuit having improved breakdown voltage characteristics; Franciscus A. C. M. Schoofs, et al., 257/256, 265, 272 [IMAGE AVAILABLE]

7. 5,394,104, Feb. 28, 1995, Power-on reset circuit including dual sense amplifiers; Napoleon W. Lee, 327/143, 77, 78 [IMAGE AVAILABLE]

8. 5,361,229, Nov. 1, 1994, Precharging bitlines for robust reading of latch data; David Chiang, et al., 365/189.05, 189.01, 189.08, 203 [IMAGE AVAILABLE]

9. 5,355,123, Oct. 11, 1994, Overheating detection circuit for detecting overheating of a power device; Masaharu Nishiura, et al., 340/653; 327/512; 340/598; 361/103; 374/152, 178 [IMAGE AVAILABLE]

10. 5,349,336, Sep. 20, 1994, Overheating detection circuit for detecting overheating of a power device; Masaharu Nishiura, et al., 340/653; 257/467; 327/512; 340/598; 361/103; 374/152, 178 [IMAGE AVAILABLE]

11. 5,239,216, Aug. 24, 1993, Clamping circuit for preventing output driving transistor from deep saturation state; Toshikazu Sei, et al., 327/314, 575, 579 [IMAGE AVAILABLE]

12. 5,239,208, Aug. 24, 1993, Constant current circuit employing transistors having specific gate dimensions; Akitoshi Tezuka, 327/427; 326/21, 121; 327/537 [IMAGE AVAILABLE]

13. 5,138,437, Aug. 11, 1992, Semiconductor integrated circuit device in which integrated circuit units having different functions are stacked in three dimensional manner; Toshio Kumamoto, et al., 257/686, 725; 361/728, 810; 439/74 [IMAGE AVAILABLE]

14. 5,016,986, May 21, 1991, Display device having an improvement in insulating between conductors connected to electronic components; Akihiro Kawashima, et al., 349/138, 150; 430/311 [IMAGE AVAILABLE]

15. 4,770,242, Sep. 13, 1988, Cooling device of semiconductor chips; Takahiro Daikoku, et al., 165/185; 257/713, 722; 361/718 [IMAGE AVAILABLE]

16. 4,627,082, Dec. 2, 1986, Semiconductor device for obtaining an accurate threshold voltage adjustment; Marcellinus J. M. Pelgrom, et al., 377/63; 257/235, 248, 250; 327/81, 581; 330/288 [IMAGE AVAILABLE]

17. 4,595,942, Jun. 17, 1986, Integrated circuit; Jan Lohstroh, 326/131, 100 [IMAGE AVAILABLE]

18. 4,532,530, Jul. 30, 1985, Bubble jet printing device; William G. Hawkins, 347/62, 64 [IMAGE AVAILABLE]

19. 4,419,745, Dec. 6, 1983, Semiconductor memory device; Kazuhiro Toyoda, et al., 365/174; 327/198; 365/156, 226 [IMAGE AVAILABLE]

20. 4,135,295, Jan. 23, 1979, Process of making platinum silicide fuse links for integrated circuit devices; William L. Price, 438/601; 29/623; 257/528, 665; 438/664 [IMAGE AVAILABLE]

21. 4,042,950, Aug. 16, 1977, Platinum silicide fuse links for integrated circuit devices; William Louis Price, 257/529; 148/DIG.20, DIG.55; 337/4, 290; 365/96 [IMAGE AVAILABLE]

22. 3,772,536, Nov. 13, 1973, DIGITAL CELL FOR LARGE SCALE INTEGRATION; Norman J. Grannis, et al., 326/38; 257/393; 326/41, 44, 102 [IMAGE AVAILABLE]

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L1         15294 S (INTEGRATED (1W) CIRCUIT?)/AB
L2            22 S L1 AND (MANUFACTUR? (2W) SAME (2W) PROCESS?)
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L3         38673 S 395/?/CCLS
L4         15294 S L1 AND (INTEGRATED (2W) CIRCUIT?)/AB

=> s l1 and (manufactur? (2w) same (2w) process? (2w) variation?)
         717681 MANUFACTUR?
        1633939 SAME
                    1124585 PROCESS?
         620474 VARIATION?
              1 MANUFACTUR? (2W) SAME (2W) PROCESS? (2W) VARIATION?
L5            0 L1 AND (MANUFACTUR? (2W) SAME (2W) PROCESS? (2W) VARIATION?)

=> s l1 and ((manufactur? (2w) same (2w) process?) (p) (temperatur? and variati
on?))
PROXIMITY OPERATION NOT ALLOWED

=> s l1 and (manufactur? (2w) smae (2w) process? (p) temperatur? (p) vari?)
         717681 MANUFACTUR?
            146 SMAE
           1124585 PROCESS?
            815810 TEMPERATUR?
              1206185 VARI?
              0 MANUFACTUR? (2W) SMAE (2W) PROCESS? (P) TEMPERATUR? (P) VARI?
L6            0 L1 AND (MANUFACTUR? (2W) SMAE (2W) PROCESS? (P) TEMPERATUR? (P
               ) VARI?)

=> s l1 and (manufactur? (2w) same (2w) process? (p) temperature? (p) vari?)
         717681 MANUFACTUR?
        1633939 SAME
                    1124585 PROCESS?
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            815805 TEMPERATURE?
              1206185 VARI?
            3 MANUFACTUR? (2W) SAME (2W) PROCESS? (P) TEMPERATURE? (P) VARI?
L7          0 L1 AND (MANUFACTUR? (2W) SAME (2W) PROCESS? (P) TEMPERATURE? (
              P) VARI?)

=>
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